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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,569	02/24/2004	Craig C. Andrews	LYNN/0094.B	9862

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,569	ANDREWS, CRAIG C.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/10/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 16 is objected to because of the following informalities: A minor spelling error occurs in Claim 16. The word ""provie" found in line 2 of Claim 16 should be changed to --provide--. Appropriate correction is required.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 14-16 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-3 of prior U.S. Patent No. 6,324,042. This is a double patenting rejection.

4. With regard to the claims, Claims 14, 15 & 16 of the pending application, are duplicates of Claims 1, 2 & 3 respectively of US Patent 6,324,042 and therefore are not further treated on the merits in this action.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1, 2, 4, 8 &17 are rejected under 35 U.S.C. 102(b) as being anticipated by Krinsky (US 5,200,692).

7. With regard to Claim 1, Krinsky, in Figure 1, discloses an apparatus for limiting current through a plurality of parallel transistors, the apparatus comprising: a means for sensing one or more operational parameters of a field effect transistor in the load (12); and means for adjusting the current through the field effect transistor in response to the one or more sensed parameters to prevent the transistor from operating outside its safe operating area (column 2 lines 2-20).

8. With regard to Claim 2, Krinsky, in Figure 3, discloses the circuit of Claim 1, wherein the parameter comprises operating current of the field effect transistor.

In the circuit taught by Krinsky, the operational amplifier (30') senses the operating current through FET 34' by feeding the voltage across sense resistor R_s' to the inverting input of the opamp (30') (column 5 lines 37-68).

9. With regard to Claim 4, Krinsky, in Figure 3, discloses the circuit of claim 1, further comprising: a means for sensing one or more operational parameters of each of the plurality of field effect transistors in the load individually; and a means for adjusting the current through each of the plurality of field effect transistors individually in response to the respective one or more sensed parameters.

Fig. 3 teaches that each FET (34') has an individual opamp (30') to sense the current of each FET separately, and each individual opamp further adjusts the FET individually.

10. With regard to Claim 8, Krinsky, in Figure 3, discloses the circuit of claim 1, wherein the means for sensing is an operational amplifier (30'), which is an active component.

11. With regard to Claim 17, Krinsky, in Figure 3, discloses a system including a plurality of field effect transistors (34') coupled in parallel to define a load, a method of protecting the field effect transistors comprising the steps of sensing one or more operational parameters of each of the field effect transistors, and modifying a control signal (column 2 lines 2-20).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 3, 5-7 & 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Krinsky as applied to claims 1, 2, 4, 8 & 17 above, and further in view of Mitter (US 5,684,663).

14. With regard to Claims 3 & 9, Krinsky teaches the circuit of Claim 1.

Krinsky does not teach that the parameter comprises a temperature associated with the field effect transistor or that the means for sensing comprises a resistor having a predetermined temperature coefficient.

Mitter, in Figure 1, teaches a protective element and method for protecting a circuit wherein a voltage divider is placed across the gate of a FET (25). The two resistors (21 & 23) of the voltage divider have a predetermined positive temperature coefficient wherein the resistors are passive elements that sense the temperature of the FET (25) (column 2 lines 44-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krinsky with Mitter, by replacing the active current sensing circuit of Fig. 3 taught by Krinsky with the passive circuit taught

by Mitter, for the purpose of reducing the size and complexity of the circuit and thus the cost while also increasing the circuits robustness.

15. With regard to Claim 5, Krinsky discloses the circuit of Claim 1. Mitter further discloses that the means for sensing can be a passive component having a characteristic parameter that is a function of the operational parameter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to combine the teachings of Krinsky and Mitter for the reasons given above for Claim 3.

16. With regard to Claim 6, Krinsky in view of Mitter discloses the circuit of Claim 5. Mitter further discloses that one or more operational parameters is temperature (column 2 lines 44-67).

17. With regard to Claim 7, Krinsky in view of Mitter discloses the circuit of Claim 5. Mitter further discloses that one of the operational parameters is current. Applicant teaches in paragraphs 22 & 23 of the disclosure that resistors with a PTC, coupled to the gate of a FET, can increase resistance upon increase in temperature or current. Thus the PTC resistors (21 & 23) taught by Mitter can also sense current.

18. Claims 10 –13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krinsky as applied to claims 1, 2, 4, 8 & 17 above, and further in view of Cisar et al. (US 5,512,831).

19. With regard to Claim 10, Krinsky teaches the circuit of Claim 1.

Krinsky does not teach that the circuit further comprises an analog feedback loop in the load whose output changes with changes in the resistance of the load.

Cisar et al., in Figure 2, teaches an analog feedback loop in the load whose output changes with changes in the resistance of the load (column 5 lines 11-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Krinsky with Cisar et al., by replacing the feed back circuit taught by Krinsky (15, 16, 18, 20,22 & 23-25) with the feedback circuit taught by Cisar et al., for the purpose of removing the Hall effect current probe (46) taught by Krinsky used for sensing the current of the load, thus removing the need for extra wiring and reducing noise from the system picked up from the wiring.

20. With regard to Claim 11, Krinsky in view of Cisar et al. discloses the circuit of Claim 10. Cisar et al further discloses that the feedback loop comprises: a. a shunt (24) in series with the load (25); an operational amplifier (26) having its inverting input coupled to one end of the shunt (24); and the non-inverting input of the operational amplifier coupled to a voltage source referenced to the other end of the shunt.

21. With regard to Claim 12, Krinsky in view of Cisar et al. discloses the circuit of Claim 11. Cisar et al. further discloses that the output of the operational amplifier provides a control signal to the gates of the field effect transistors of the load (column 5 lines 11-27).

22. With regard to Claim 13, Krinsky in view of Cisar et al. discloses the circuit of Claim 10. Cisar et al. further discloses that the circuit further comprising a digital programmable device (28 & 30) providing a control signal (32 & 34) to the analog feedback loop to alter the operation of the feedback loop.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB
26 JAN 2006

PHUONG T. VU
PRIMARY EXAMINER